Cisco Nexus K3P-Q FPGA SmartNIC

Contents

High-density, ultra-low latency network interface card

The Cisco Nexus K3P-Q FPGA SmartNIC is a high-density SmartNIC, specifically optimized for low latency operation.

Features 2x QSFP28 ports that can be deployed in a high-density 8-channel configuration and software trigger-to-response latencies as low as 596ns. This is up to 20 percent faster than previous Cisco Nexus SmartNIC models, making it one of the fastest high-density network adapters in the market. Users will find that this drop-in replacement SmartNIC accelerates tick-to-trade performance to previously unachievable speeds, increasing the efficiency and profitability of software-based trading systems.

Advanced software programmability

The Cisco Nexus K3P-Q FPGA SmartNIC provides the most powerful programmable software interface on the market.

Programmability features include:

- Zero-latency cost hardware flow steering: allowing traffic filtering and steering to the right memory and CPU core with no latency penalty.
- Cut-through receive: Allows software to process packet fragments as they arrive from the wire, while packet tails are still in flight. Especially effective for slow line speeds (for example, 1GbE). The Cisco Nexus K3P-Q FPGA SmartNIC software API puts users well ahead of traditional store-and-forward SmartNIC designs to make better decisions faster.
- ExaSOCK TCP/IP acceleration: Unmodified socket applications benefit from the speed and power of the Cisco Nexus K3P-Q FPGA SmartNIC using ExaSOCK's in-place TCP/IP socket acceleration system. ExaSOCK's Extension API allows it to seamlessly interoperate with the Nexus K3P-Q SmartNIC's transmit preloading feature, as described below.
- Preloaded packet transmit: The Cisco Nexus K3P-Q FPGA SmartNIC allows users to preload transmit frames, saving 60ns from the transmit path. The Cisco Nexus K3P-Q FPGA SmartNIC features enlarged packet transmit buffers allowing many more frames to be preloaded, leading to more versatile transmission choices.
- High-resolution timestamps: Four-nanosecond timestamps are applied to every received packet and the most recently transmitted packet. The Cisco Nexus K3P-Q FPGA SmartNIC also features out of the box support for IEEE1588 (PTP) and high-speed capture to disk using free and open-source Exact-Capture software.

25GbE[4] ready

The Cisco Nexus K3P-Q FPGA SmartNIC is a pure FPGA-based network adapter that is 25GbE ready.

FPGA (Field Programmable Gare Array) design extends the useful life of the Cisco Nexus K3P-Q FPGA SmartNIC by allowing new features and speed enhancements to be downloaded into the adapter after deployment. For example, the Cisco Nexus K3P-Q FPGA SmartNIC will support additional Ethernet speeds through a firmware update. This will reduce capital expenditure on lengthy and difficult infrastructure upgrades.

All-FPGA design

The Cisco Nexus K3P-Q FPGA SmartNIC is built using the latest generation Xilinx UltraScale+ FPGA

The SmartNIC optionally ships with 9GB of DDR4 memory for custom applications, and it is a compact low-profile form-factor adapter. The all-FPGA design allows the user to offload critical network processing functions directly into the SmartNIC, while maintaining the ease of use and administration of a production-grade network adapter.

Figure 1.
Cisco Nexus K3P-Q FPGA SmartNIC

Performance

Typical latency, raw frames:[1]

- 64 bytes: 714 ns
- 256 bytes: 927 ns

Typical latency, raw frames with preloaded TX buffer:[1]

- 64 bytes: 653 ns
- 256 bytes: 690 ns

Typical latency, UDP:[2]

- 14 bytes: 828 ns
- 256 bytes: 1.11 µs

Typical latency, TCP:[2]

- 14 bytes: 869 ns
- 256 bytes: 1.13 µs

Timestamping

Timestamp resolution:

- 4ns

Timestamp availability:

- All received frames, most recently transmitted frame

Time synchronization:

- Host, hardware assisted PTP, optional PPS

PPS input/output:

- 3.3V CMOS, selectable 50ohm termination

Other features

Capture:

- Line-rate capture to disk

Flow steering:

- 256 IP rules per port
- 64 MAC rules per port

FPGA Development Kit:

- Add custom user logic to FPGA
- Fully integrated with drivers and utilities
- Xilinx Ultrascale+ XCKU3P-2
- 9GB DDR4 (optional)

General

Form factor:

- Low-profile PCI Express Card
- 117x68mm (4.65x2.67in)

Environmental:

- Operating temperature: 0 °C to 55 °C
- Storage temperature: -40 °C to 70 °C
- Operating Relative Humidity: 5% to 90% (non-condensing)
- Storage Relative Humidity: 5% to 95% (non-condensing)

Recovery:

- Manual firmware recovery button

Ports:

- 2x QSFP28
- SMA for PPS in/out

Data rates:

- 40GbE, 25GbE[3], 10GbE, 1GbE, 100M Fast Ethernet

Supported media:

- Fiber (40/100GBASE-SR4, 40/100GBASE-LR4), QSFP(+/28) Direct Attach

Host interface:

- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Operating systems:

- Linux x86_64 (all distributions)

Product sustainability

Information about Cisco's environmental, social, and governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability reporting.

Table 1. Cisco environmental sustainability information

Sustainability topic		Reference
General	Information on product-material-content laws and regulations	Materials
	Information on electronic waste laws and regulations, including our products, batteries, and packaging	WEEE Compliance
	Information on product takeback and reuse program	Cisco Takeback and Reuse Program
	Sustainability inquiries	Contact: csr_inquiries@cisco.com
	Environmental	General
Material	Product packaging weight and materials	Contact: environment@cisco.com
	Form factor	General

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Footnote

1. Latencies are median latencies for raw frames from wire-userspace-wire via the libexanic, on a 3.5Ghz Intel® Ivy Bridge processor.

2. Latencies are median half-roundtrip time latencies for the sockperf benchmark using the exasock socket acceleration library. More information about benchmarking methodology is available on request.

3. Future Firmware release

4. QSFP ports are initially used as 4x10G logical ports, future firmware releases will enable the support for 25G per lane for 4x25G mode

Americas Headquarters
Cisco Systems, Inc.
San Jose, CA

Asia Pacific Headquarters
Cisco Systems (USA) Pte. Ltd.
Singapore

Europe Headquarters
Cisco Systems International BV Amsterdam,
The Netherlands

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